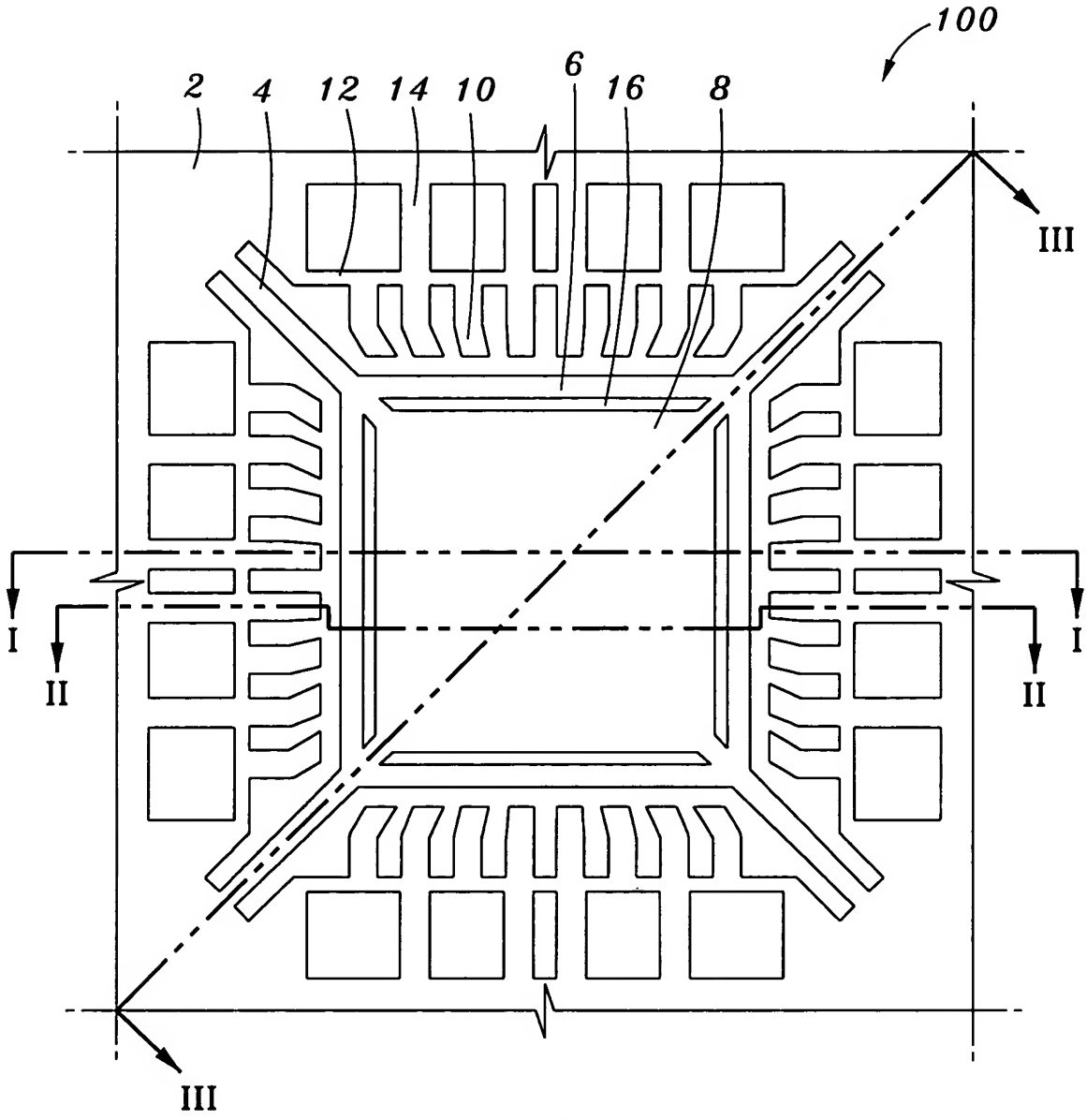

FIG. 1

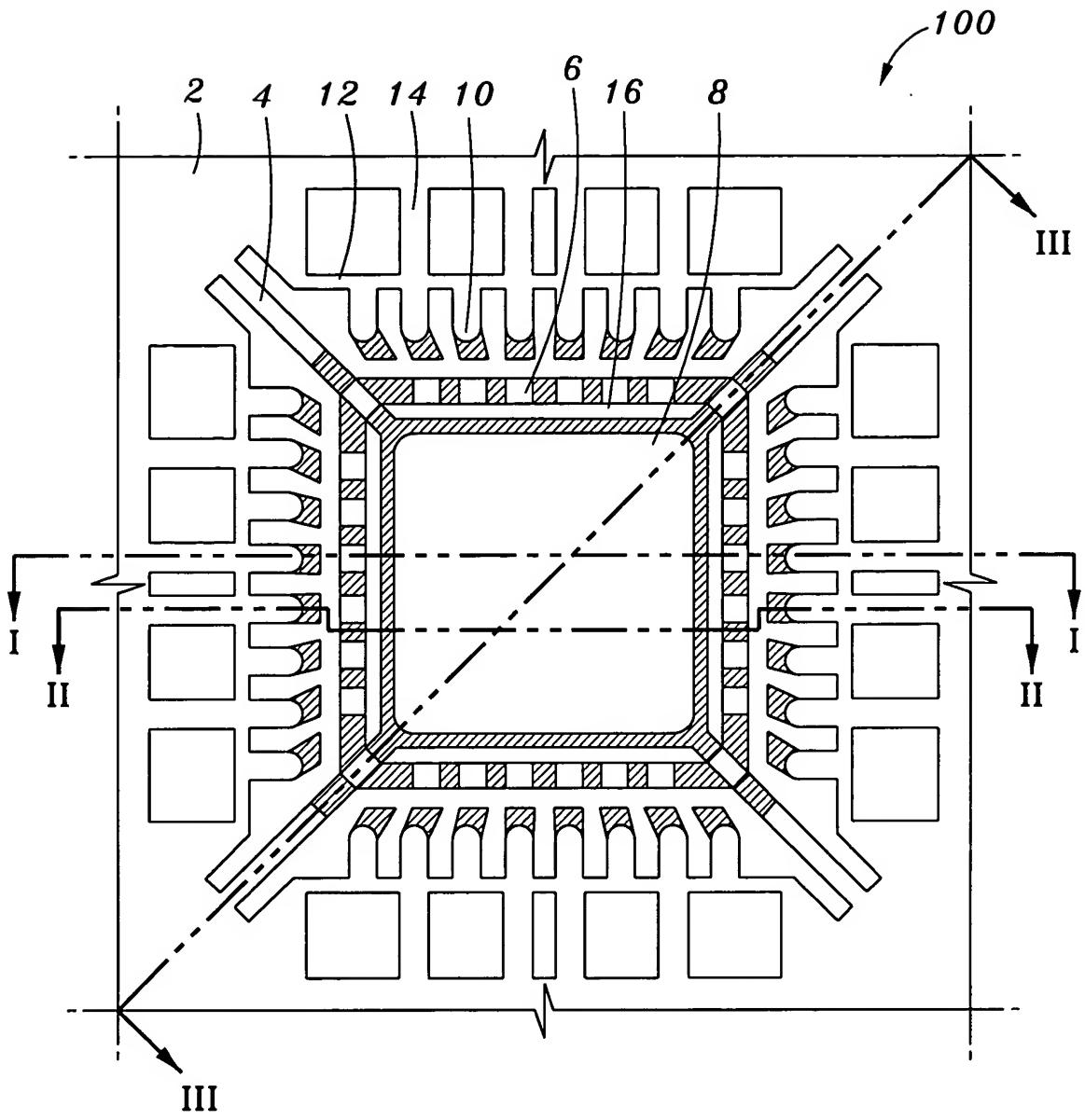

FIG. 2

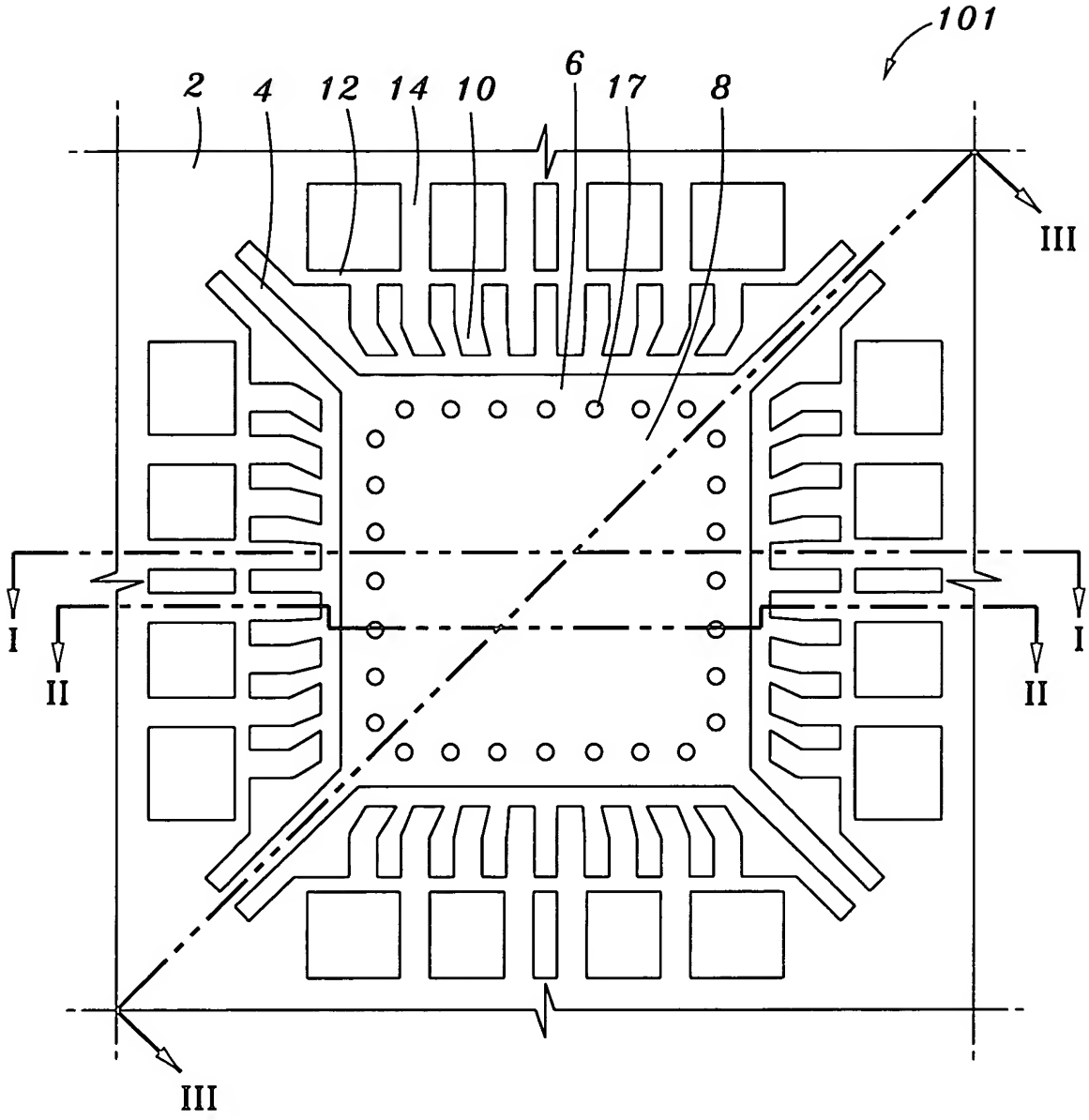

FIG. 3

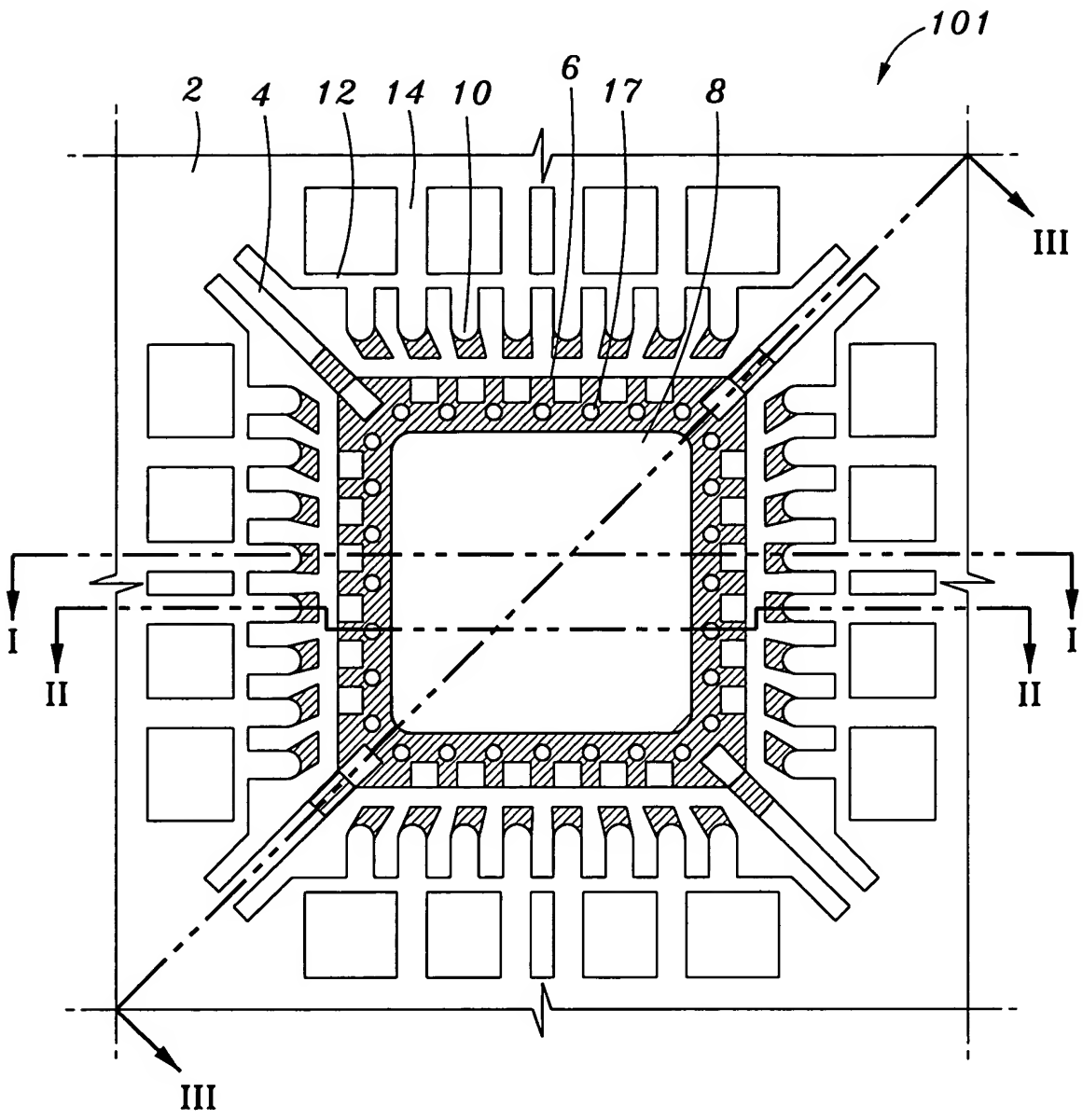

FIG. 4

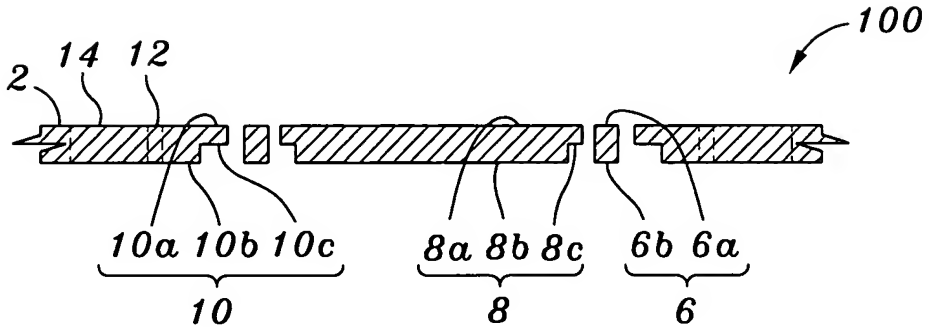

FIG. 5

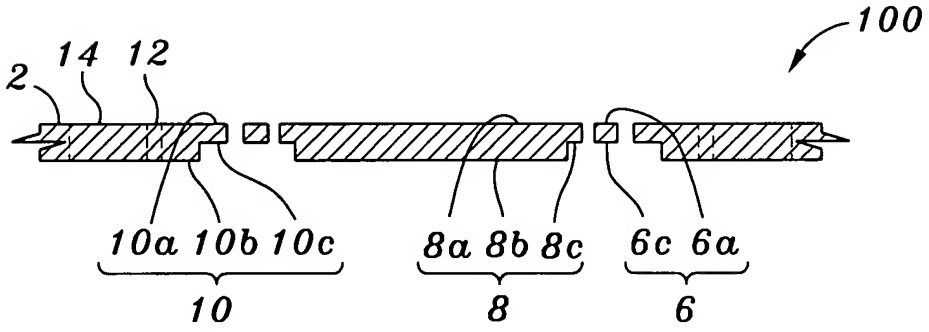

FIG. 6

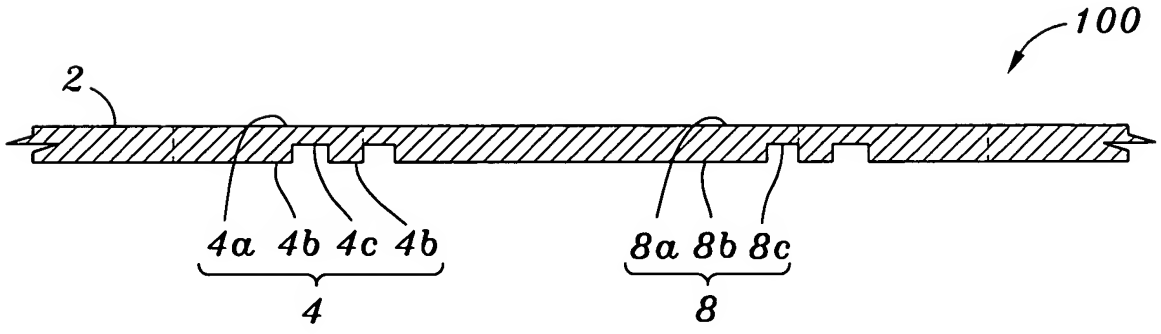

FIG. 7

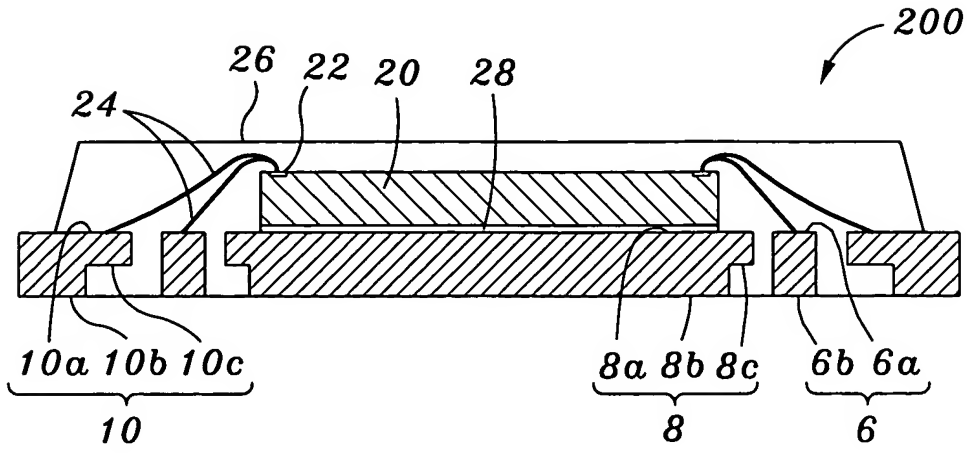

FIG. 8

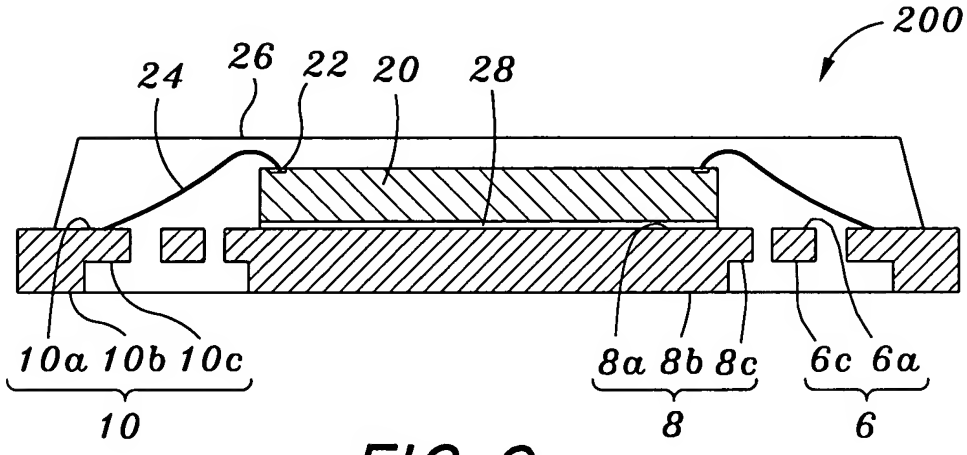

FIG. 9

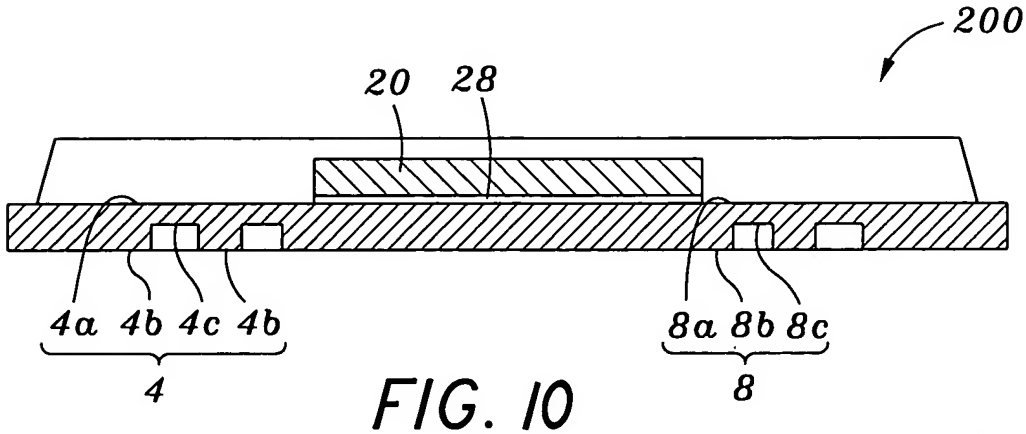

FIG. 10

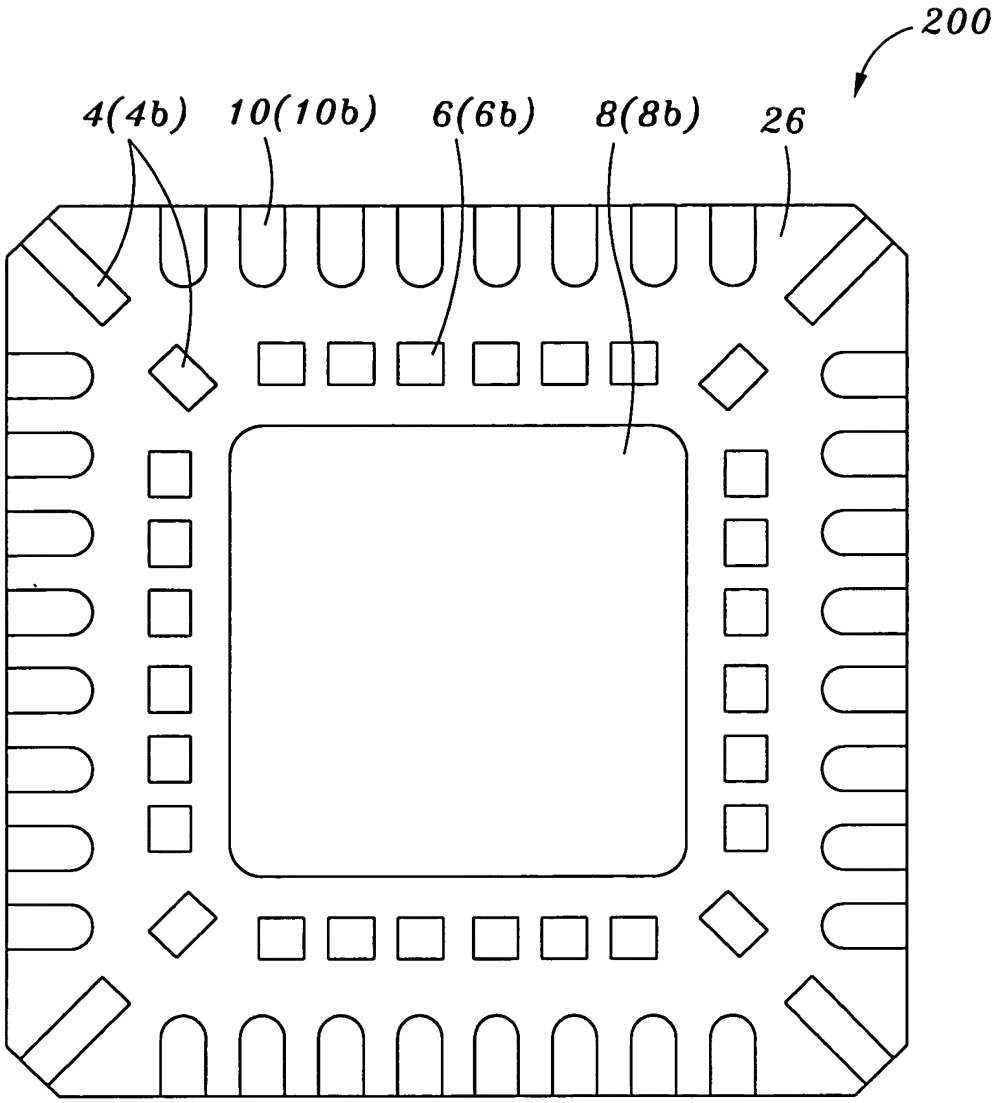

FIG. II

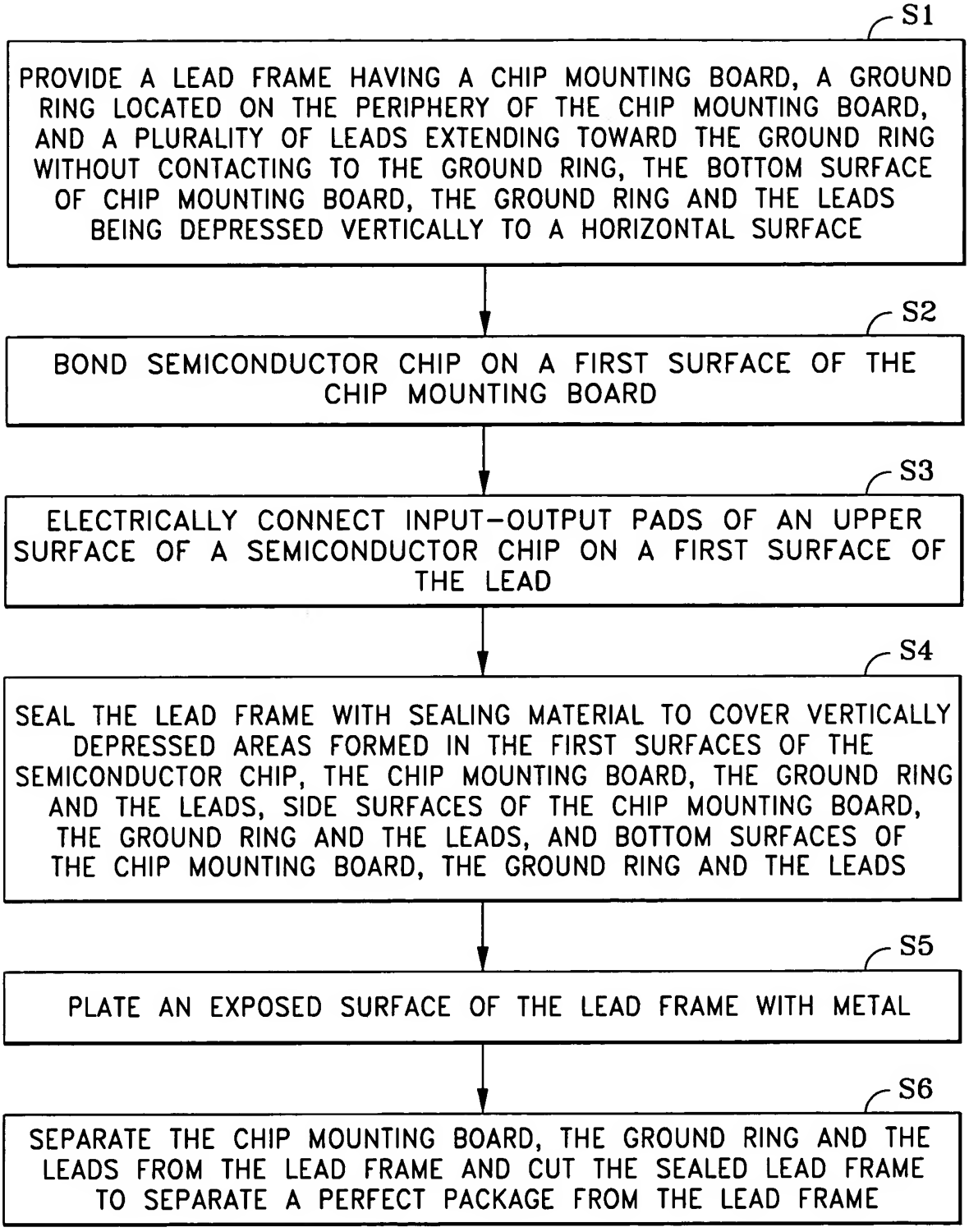
S1
PROVIDE A LEAD FRAME HAVING A CHIP MOUNTING BOARD, A GROUND RING LOCATED ON THE PERIPHERY OF THE CHIP MOUNTING BOARD, AND A PLURALITY OF LEADS EXTENDING TOWARD THE GROUND RING WITHOUT CONTACTING TO THE GROUND RING, THE BOTTOM SURFACE OF CHIP MOUNTING BOARD, THE GROUND RING AND THE LEADS BEING DEPRESSED VERTICALLY TO A HORIZONTAL SURFACE
S2
BOND SEMICONDUCTOR CHIP ON A FIRST SURFACE OF THE CHIP MOUNTING BOARD
S3
ELECTRICALLY CONNECT INPUT-OUTPUT PADS OF AN UPPER SURFACE OF A SEMICONDUCTOR CHIP ON A FIRST SURFACE OF THE LEAD
S4
SEAL THE LEAD FRAME WITH SEALING MATERIAL TO COVER VERTICALLY DEPRESSED AREAS FORMED IN THE FIRST SURFACES OF THE SEMICONDUCTOR CHIP, THE CHIP MOUNTING BOARD, THE GROUND RING AND THE LEADS, SIDE SURFACES OF THE CHIP MOUNTING BOARD, THE GROUND RING AND THE LEADS, AND BOTTOM SURFACES OF THE CHIP MOUNTING BOARD, THE GROUND RING AND THE LEADS
S5
PLATE AN EXPOSED SURFACE OF THE LEAD FRAME WITH METAL
S6
SEPARATE THE CHIP MOUNTING BOARD, THE GROUND RING AND THE LEADS FROM THE LEAD FRAME AND CUT THE SEALED LEAD FRAME TO SEPARATE A PERFECT PACKAGE FROM THE LEAD FRAME

FIG. 12

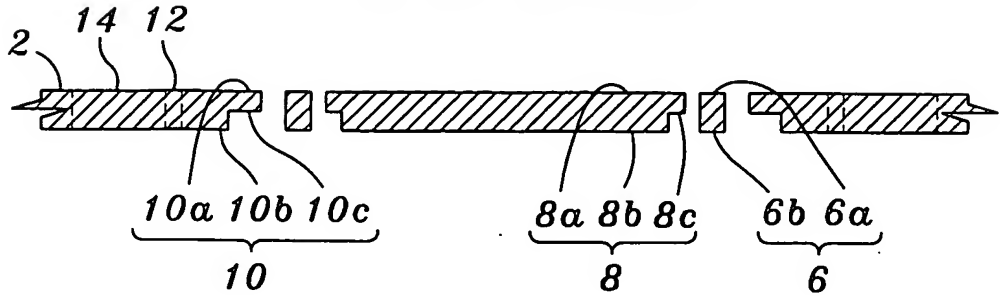

FIG. 13

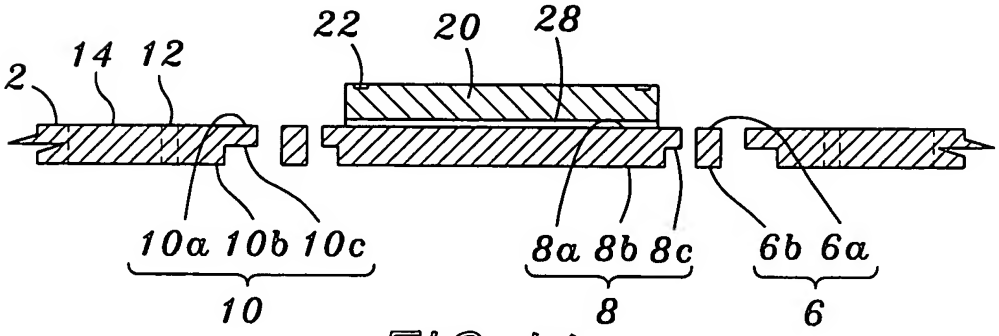

FIG. 14

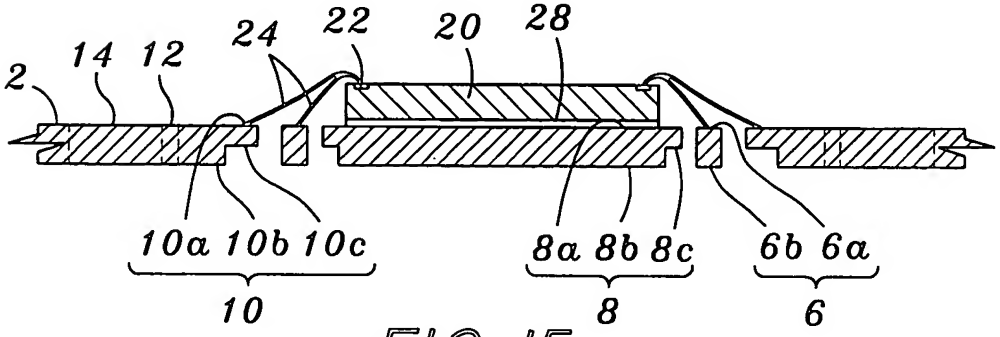

FIG. 15

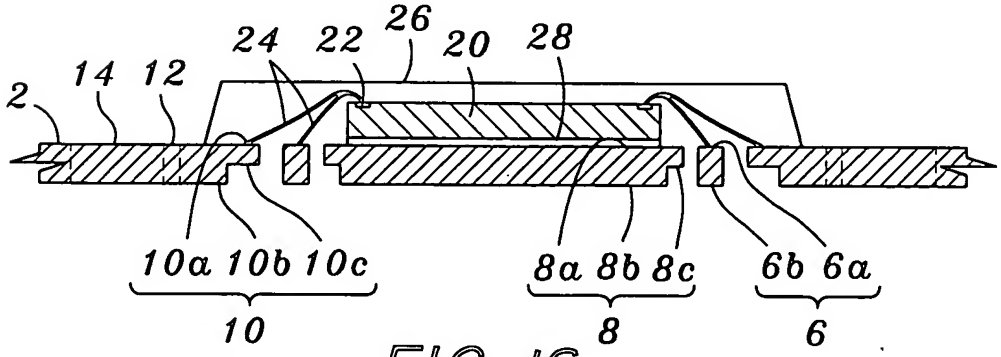

FIG. 16

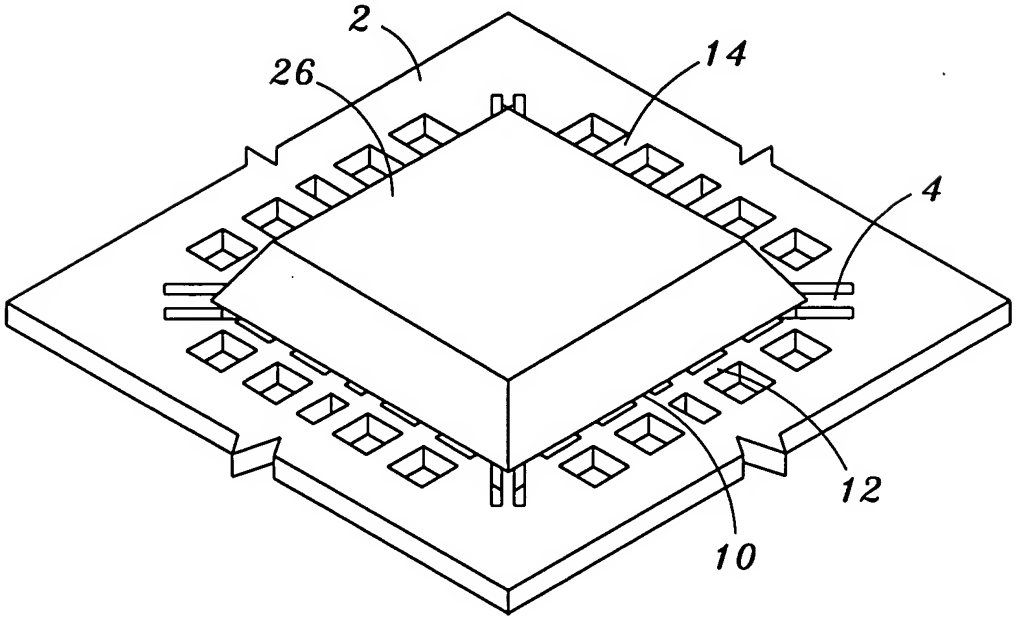

FIG. 17

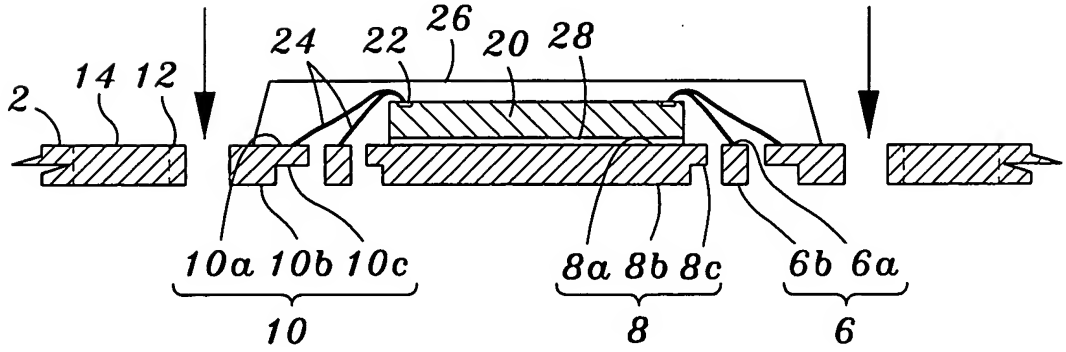

FIG. 18